SEMESTER S6

VLSI VERIFICATION

Course Code	PEEVT 632	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3-0-0-0	ESE Marks	60
Credits	3	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	PBECT304	Course Type	Theory

Course Objectives:

This Course aims to impart the knowledge of

1. The fault modelling and fault detection.
2. The concepts of test generation for combinational circuits
3. The concepts of test generation methods – DFT, BIST.
4. concepts of fault diagnosis

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Introduction, VLSI design flow, need of Pre-silicon verification and post-silicon validation and debug -Role of Testing -Yield-ATE. Fault Modelling - single stuck-at-faults, Bridging faults, delay faults -functional equivalence and fault collapsing, Dominance collapsing and check point theorem. Logic and Fault Simulation - serial and parallel fault simulation.	9
2	Testability Measures- Combinational Controllability - Combinational Observability. Combinational ATPG-Path sensitization method , Boolean Difference Method-D-Algorithm-PODEM	9
3	Design for Testability – DFT Fundamentals, Scan design, Partial Scan, Random Access Scan	9
4	BIST- LFSR Pattern Generation-Output Response Analysis-BILBO. Boundary Scan standard. Introduction to Formal Design Verification. Introduction to Fault Diagnosis and Self-checking design.	9

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	15	10	10	40

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

	Course Outcome	Bloom's Knowledge Level (KL)
CO1	Apply Fault equivalence and Fault collapsing	**KL3**
CO2	Apply basic ATPG Algorithms used in VLSI Testing.	**KL3**
CO3	Explain the concept of DFT	**KL2**
CO4	Apply BIST for output response analysis	**KL3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**3**	**3**										**2**
CO2	**3**	**3**										**2**
CO3	**3**	**3**										**2**
CO4	**3**	**3**										**2**

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Essentials of Electronic Testing of Digital Memory and Mixed Signal VLSI Circuits	Viswani D Agarwal and Michael L Bushnell	Kluwer Academic Publishers	2000

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	High-Level Synthesis: Introduction to Chip and System Design	D. D. Gajski, N. D. Dutt, A.C.-H. Wu and S.Y.-L. Lin	Springer	1st edition, 1992.
2	Digital systems Testing and Testable Design	M. Abramovici, M A Breuer and A D Friedman	IEEE Press	1994
3	Testing of Digital Systems	Niraj Jha and Sanjeep K Gupta	Cambridge University Press	2003
4	Digital Circuit Testing and Testability	P.K. Lala	Academic Press	2002

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://youtu.be/kW70cVmWSR8?si=B0u137fAG1Nrzu7X
2	https://youtu.be/zekvZgaK54o?si=wU-Uiu8LucspC7W4
3	https://youtu.be/FBjTy-JMZ8Y?si=7tU4qs353srSPjsg
4	https://youtu.be/5jBAVSN_U0g?si=tGa7U4OjiiojAYfw